**第五章习题答案**

**5.1 F = [ (AB’C’) (B’C’D’)’ ] = AB’C’ + B’C’D’ 真值表略**

**5.2 （1） 0**

**ABD**

**C**

**Y1**

**C‘**

**Y2**

**Y**

**（2）A=B=D时，C从1->0或0->1变化时，可能产生冒险**

**（3）利用卡诺图分析得：F=（C+D）（A+B+C’）（A+B+D）**

**5.3**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **AB**  **CD** | **00** | **01** | **11** | **10** |
| **00** | **1** | **1** | **1** |  |
| **01** | **1** | **1** | **1** |  |
| **11** |  |  | **1** |  |
| **10** |  |  | **1** |  |

**5.4（1）1F= AB’C + B’ + B’D’ + B’C’ + A’D’**

**（2）F =**

**= AC’D’ + ABD + B’CD + AB’C**

**= [(AC’D’)’(ABD)’(B’CD)’(AB’C)’]’**

**5.5真值表：卡诺图：**

**A B C F**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **AB**  **C** | **00** | **01** | **11** | **10** |
| **0** | **1** |  | **1** |  |
| **1** |  | **1** | **1** | **1** |

**0 0 0 1**

**0 0 1 0**

**0 1 0 0**

**0 1 1 1**

**1 0 0 0**

**1 0 1 1**

**1 1 0 1 F = A’B’C’ + AB + BC + A’C**

**1 1 1 1**

**5.6 真值表：卡诺图：**

**M A B C F**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **MA**  **BC** | **00** | **01** | **11** | **10** |
| **00** |  |  |  | **1** |
| **01** |  | **1** |  |  |
| **11** | **1** | **1** | **1** |  |
| **10** |  | **1** |  |  |

**0 0 0 0 0**

**0 0 0 1 0**

**0 0 1 0 0**

**0 0 1 1 1**

**0 1 0 0 0**

**0 1 0 1 1**

**0 1 1 0 1**

**0 1 1 1 1**

**1 0 0 0 1**

**1 0 0 1 0**

**1 0 1 0 0 F=MA’B’C’+M’AB+M’AC+M’BC+ABC**

**1 0 1 1 0 两级与非门：**

**1 1 0 0 0 F=[(MA’B’C’)’ (M’AB)’ (M’AC)’ (M’BC)’ (ABC)’]’**

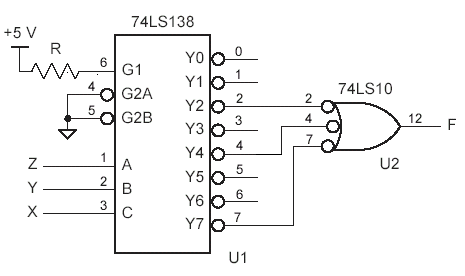
**1 1 0 1 0**

**1 1 1 0 0**

**1 1 1 1 1**

**5.7 指出用一块或多块74X138或74X139二进制译码器以及与非门，如何构建下面每个单输出或多输出的逻辑功能（提示：每个实现等效于一个最小项之和）**

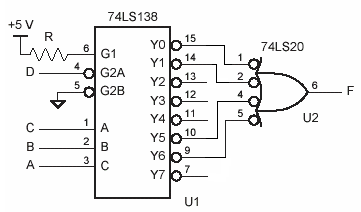
**解：（1）F=**

****

**（2）F =**



**（3）F =**



**5.8 真值表：（1）**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **AB**  **C** | **00** | **01** | **11** | **10** |
| **0** |  |  | **1** |  |
| **1** |  | **1** | **1** | **1** |

**A B C Y Z Y**

**0 0 0 0 0**

**0 0 1 0 1**

**0 1 0 0 1**

**0 1 1 1 0**

**1 0 0 0 1**

**1 0 1 1 0 Y = AB + BC + AC**

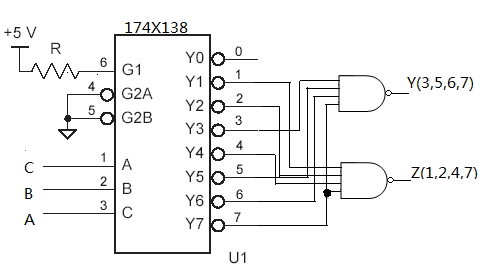
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **AB**  **C** | **00** | **01** | **11** | **10** |
| **0** |  | **1** |  | **1** |
| **1** | **1** |  | **1** |  |

**1 1 0 1 0Z**

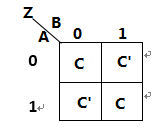
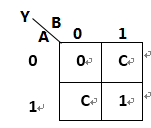
**1 1 1 1 1**

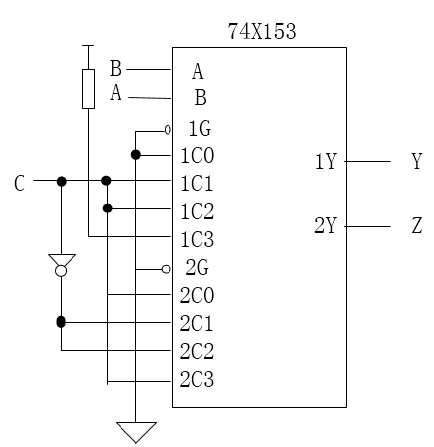
**Z = A’B’C + A’BC’ + AB’C’ + ABC**

**（2）**

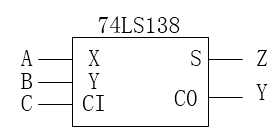
****

**（3）**



****

**（4）Y = AB + AC + BC**



**5.9 解：该电路中两个2-4译码器同时使能，会导致2个3态门同时导通，出现逻辑电平冲突。为解决这一问题，在EN\_L至1G（或2G）的线路上加一个反相器，使两路门不可能同时导通。**

**5.10 奇校验**

**5.11 解：**

**5.12**

**A1 B1 A2 B2 Y1 Y2 A1 B1 A2 B2 Y1 Y2**

**0 0 0 0 0 0 1 0 0 0 0 0**

**0 0 0 1 0 0 1 0 0 1 0 0**

**0 0 1 0 0 0 1 0 1 0 0 0**

**0 0 1 1 0 1 1 0 1 1 0 1**

**0 1 0 0 0 0 1 1 0 0 1 0**

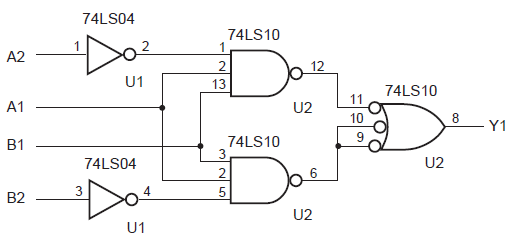
**0 1 0 1 0 0 1 1 0 1 1 0**

**0 1 1 0 0 0 1 1 1 0 1 0**

**0 1 1 1 0 1 1 1 1 1 0 0**

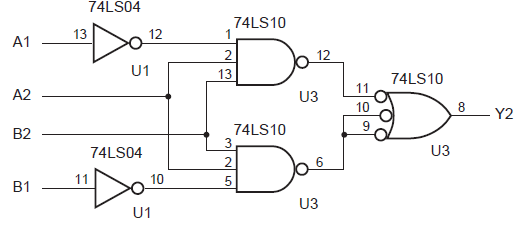
**Y1**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A1B1**  **A2B2** | **00** | **01** | **11** | **10** |
| **00** |  |  | **1** |  |
| **01** |  |  | **1** | **1** |
| **11** |  |  |  |  |
| **10** |  |  | **1** |  |



**Y2**

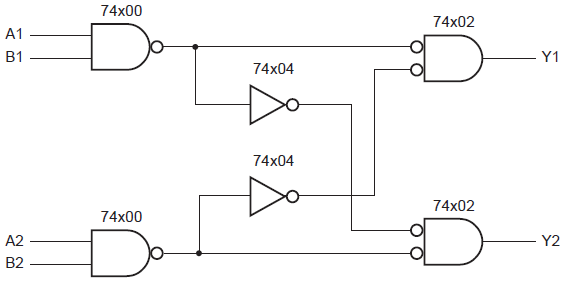
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A1B1**  **A2B2** | **00** | **01** | **11** | **10** |
| **00** |  |  |  |  |
| **01** |  |  |  |  |
| **11** | **1** | **1** |  | **1** |
| **10** |  |  |  |  |

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**5.13**

解：CMOS晶体管用量：反相器2个，2输入与非门4个，3输入与非门6个

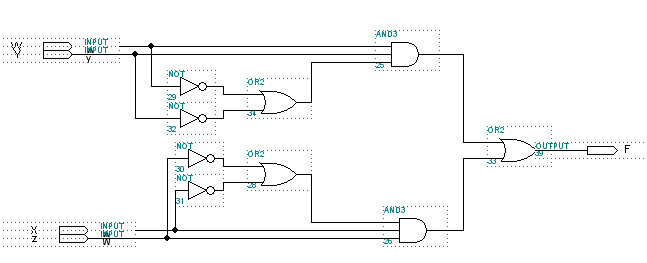
晶体管用量：20只（原设计中晶体管用量为40只）

****

**5.14**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **WX**  **YZ** | **00** | **01** | **11** | **10** |
| **00** |  |  |  |  |
| **01** |  | **1** | **1** |  |
| **11** |  | **1** |  | **1** |
| **10** |  |  | **1** | **1** |

**F=W’XZ+XY’Z+WX’Y+WYZ’**

****

**5.15解：真值表为：**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 | Y9 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | d | d | d | d | d | d | d | d | d | d |
| 1 | 0 | 1 | 1 | d | d | d | d | d | d | d | d | d | d |
| 1 | 1 | 0 | 0 | d | d | d | d | d | d | d | d | d | d |
| 1 | 1 | 0 | 1 | d | d | d | d | d | d | d | d | d | d |
| 1 | 1 | 1 | 0 | d | d | d | d | d | d | d | d | d | d |
| 1 | 1 | 1 | 1 | d | d | d | d | d | d | d | d | d | d |

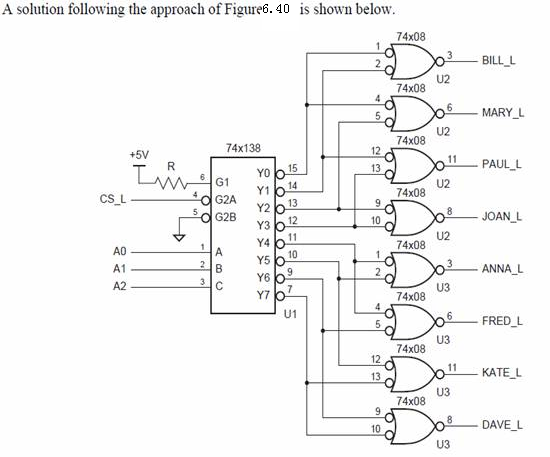
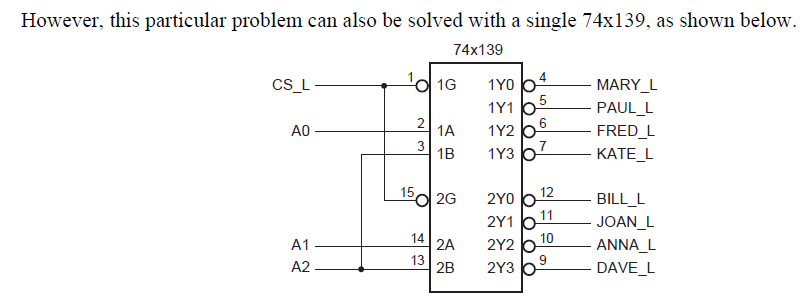
利用卡诺图化简可得：

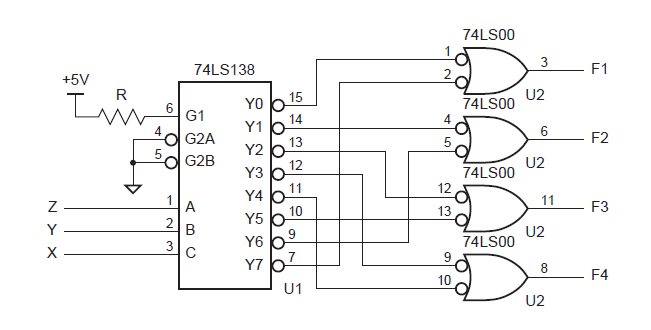






**5.16**

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**5.17**

**5.18**

module vr7seg(A,B,C,D,EN,SEGA,SEGB,SEGC,SEGD,SEGE,SEGF,SEGG);

input A,B,C,D,EN;

output SEGA,SEGB,SEGC,SEGD,SEGE,SEGF,SEGG;

reg SEGA,SEGB,SEGC,SEGD,SEGE,SEGF,SEGG;

reg [1:7] SEGS;

always @(A or B or C or D or EN)

begin

if (EN)

case ({D,C,B,A})

//Segment patterns abcdefg

0:SEGS=7'b1111110; //0

1:SEGS=7'b0110000; //1

2:SEGS=7'b1101101; //2

3:SEGS=7'b1111001; //3

4:SEGS=7'b0110011; //4

5:SEGS=7'b1011011; //5

6:SEGS=7'b1011111; //6('tail')

7:SEGS=7'b1110000; //7

8:SEGS=7'b1111111; //8

9:SEGS=7'b1111011; //9('tail')

default SEGS=7'b1001111; (“E”)

endcase

else SEGS=7'b0;

{SEGA,SEGB,SEGC,SEGD,SEGE,SEGF,SEGG}=SEGS;

end

endmodule

**5.19**

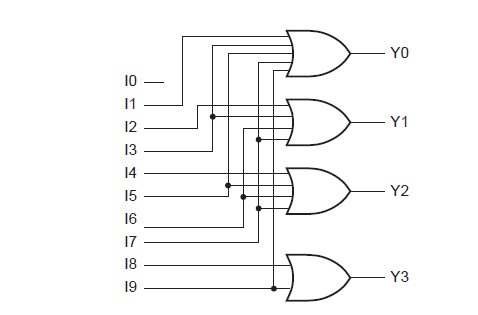
**解：简化真值表为：**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Y3** | **Y2** | **Y1** | **Y0** |  |  | **Y3** | **Y2** | **Y1** | **Y0** |
| **0** | **0** | **0** | **0** | **0** |  | **5** | **0** | **1** | **0** | **1** |
| **1** | **0** | **0** | **0** | **1** |  | **6** | **0** | **1** | **1** | **0** |
| **2** | **0** | **0** | **1** | **0** |  | **7** | **0** | **1** | **1** | **1** |
| **3** | **0** | **0** | **1** | **1** |  | **8** | **1** | **1** | **0** | **0** |
| **4** | **0** | **1** | **0** | **0** |  | **9** | **1** | **1** | **1** | **1** |

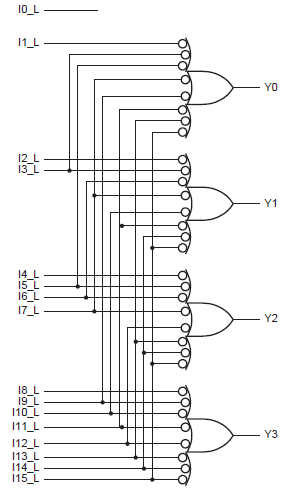
**可得：Y3=I9+I8**

**Y2= I9+I8+I7+I6+I5+I4**

**Y1= I9+I7+I6+I3+I2**

**Y0=I9+I7+I5+I3+I1**

**5.20**

**解：在此电路中，输入低电平有效且输出为高电平。**

**5.21**

**解：IN从高态到低态：有3个与非门从低态到高态，而另外3个与非门从高态到低态。**

**由于与非门,所以对单个门采用最坏情况的延迟量进行计算，结果不变。**

**5.22解：**

**74LS86 2级与3级的区别：**

**当一个输入为低电平，另一个输入变化，此时经过2个与非门传递，对应74LS86 2级的参数；当一个输入为高电平，另一个输入变化，此时经过3个与非门传递，对应74LS86 3级的参数。**

**IN从0到1：**

**IN从1到0：**

**最小延迟通常为典型值的1/4~1/3。**

**IN从0到1:**

**IN从1到0：**

**5.23**

**低电平有效输出的译码器更快, 因为反相门比非反相门更快。**